CPU-A

Headers Available
10
14
16
20
24
26
30
34
40

CPU-A

Updated V1.0 3/11/21

CPU-B connectors

CPU-B connectors

CPU-B connectors

IR7	IR6	IR5	IR4	IR3	IR2	IR1	IR0
0	0	A/F	F	F	F	D	D

2/4/2 instructions

IR7	IR6	IR5	IR4	IR3	IR2	IR1	IR0
1	1	S	S	S	D	D	D

2/3/3 instructions

Title		
Size A2	Number	Revision
Date: 29/06/2025		Sheet of
File: C:\Users\...\CPU-A.SchDoc		Drawn By:

At Load, Cap holds Select for T=RC while Hold is established.

Title	Generic 8 bit Register		
Size A3	Number		Revision
Date: 29/06/2025		Sheet of	
File: C:\Users\..\InstRegister.SchDoc		Drawn By:	

IR[7..0]
IR[7..0]
+12
IR7
IR6
IR5
IR4
IR3
IR1
IR0
IR2
K22
K23
K21
K24
K26
K27
K25
K28
K29
K30
K31
M21
M22
M20
M23
M24
M25
M26
M27
M28
M29
GND
BRA
MEM-I
MOV
SYS
ALU
FN[15..0]
FN0
FN1
FN2
FN3
FN4
FN5
FN6
FN7
FN8
FN9
FN10
FN11
FN12
FN13
FN14
FN15
SRC0
SRC1
SRC2
SRC3
SRC4
SRC5
SRC6
SRC7
FN-LEDS
CPU16LEDs.SchDoc
LED[15..0]
SRC-LEDS
CPU8LEDS.SchDoc
LED[7..0]
DEST-LEDS
CPU8LEDS.SchDoc
LED[7..0]
DES-LEDS
CPU4LEDS.SchDoc
LED[3..0]
ALU Hi order
3Bit Source Decode
SRC[7..0]
2Bit Destination Decode
DES[3..0]
3Bit Destination Decode
DEST[7..0]
DES0
DES1
DES2
DES3
DEST0
DEST4
DEST1
DEST5
DEST2
DEST6
DEST3
DEST7
000
100
001
101
010
110
011
111
R55 Res3 2k2
R56 Res3 2k2
R57 Res3 2k2
R58 Res3 2k2
R59 Res3 2k2
D55 LED3
D56 LED3
D57 LED3
D58 LED3
D59 LED3
Title
Instruction Group Decode
Size
A3
Number
Revision
Date: 29/06/2025
Sheet of
File: C:\Users\..\IR-Decode.SchDoc
Drawn By:

Title		
Size A2	Number	Revision
Date: 29/06/2025		Sheet of
File: C:\Users\...\Sequencer.SchDoc		Drawn By:

Fetch: access mem, PC, Load IR

Fetch/Increment: Load PC+

Title		
FETCH		
Size A4	Number	Revision
Date: 29/06/2025		Sheet of
File: C:\Users\..\Fetch.SchDoc		Drawn By:

After HALT, operator manual reset.
RESET instruction leaves all states except SEQ & PC board.
NOP execute Fetch and then SEQRES
WAIT0 waits for operator release via EndWait switch, or peripheral.

WAIT used with I/O

To output a Byte, write to address.

To input from External Device:

Wait(ing) is asserted,
Present Byte, LoadExt
Toggle EndWait.
CPU is then released from wait,
And Reads expected Byte.

At S1 of next Fetch Wait-Block removed.

F/A: 0=SYS, 1=ALU

ALU 2/4/2

0	0	F/A	A	A	A	D	D

0000 = HALT
0001= RESET
0010 = NOP
0011= WAIT0

1000 = ADDAB
1001 = A&B
1010 = NOTA
1011 = INCB
1100 = RORA
1101 = ROLB

A=00
B=01
C=02

Title		
Size A3	Number	Revision
Date: 29/06/2025	Sheet of	
File: C:\Users\..\SYS-1.SchDoc	Drawn By:	

MOV

2/3/3

1	1	S	S	S	D	D	D

A=000
B=001
C=010
M=011
nc=100
AD+=101
PC=110
NULL=111

A=000
B=001
C=010
MH=011
ML=100
AD+=101
PC=110
nc=111

Move Register:
MOVA,B
MOVA,C
MOVB,A
MOVB,C
MOVC,A
MOVC,B
CLRA
CLRB
CLRC

MOVA,ML
MOVA,MH
MOVB,ML
MOVB,MH
MOVC,ML
MOVC,MH

MOVAD+,PC
MOVPC,AD+
MOVM12,PC

NB. MOVPCAD+ results in incremented PC in AD+ latch.
CLRA = 11 111 000, 111 = SRC Null, 000 = dest A, F(8+Reg)

Title	MOV Registers		
Size A3	Number		Revision
Date: 29/06/2025		Sheet of	
File: C:\Users\..\MOV.SchDoc		Drawn By:	

ALU

F/A: 0=SYS, 1=ALU

ALU 2/4/2

0	0	F/A	A	A	A	D	D

AAAA = Fn

00

0000 = HALT
0001= RESET
0010 = NOP
0011= WAIT0

1000 = ADDAB
1001 = A&B
1010 = NOTA
1011 = INCB
1100 = RORA
1101 = ROLB

A=00
B=01
C=10

Title	ALU to REGS		
Size A3	Number		Revision
Date:	29/06/2025	Sheet of	
File:	C:\Users\..\ALU.SchDoc	Drawn By:	

Title		
Size A4	Number	Revision
Date: 29/06/2025		Sheet of
File: C:\Users\..\SEQ16LEDs.SchDoc		Drawn By:

Title		
Size A4	Number	Revision
Date: 29/06/2025		Sheet of
File: C:\Users\..\CPU16LEDs.SchDoc		Drawn By:

Title		
Size A4	Number	Revision
Date: 29/06/2025		Sheet of
File: C:\Users\..\CPU4LEDS.SchDoc		Drawn By:

Title		
Size A4	Number	Revision
Date: 29/06/2025		Sheet of
File: C:\Users\..\CPU8LEDS.SchDoc		Drawn By: